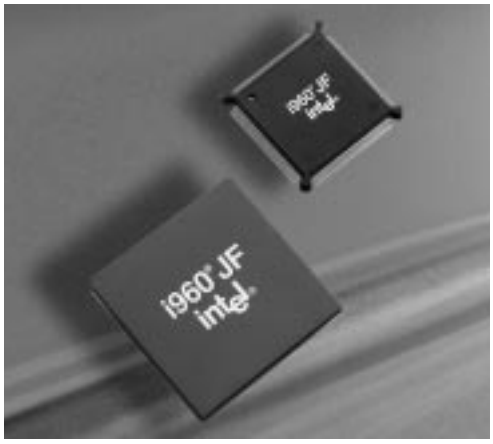
KEEPING YOU ONE DESIGN AHEAD

i960® Jx Microprocessor

The Cobra Series

PRODUCT OVERVIEW



CHOOSING A 32-BIT RISC MICROPROCESSOR

In an embedded market with increasing competition and an infinite number of product variations, the design engineer has the difficult task of choosing the best architecture for his application. Intel's i960® microprocessor family wants the customer to make an architecture choice for today and the future. Many designers have already recognized the advantages of the i960 architecture as seen by the i960 microprocessor family's position as the leading seller in the 32-bit RISC market for 1992, 1993, and 1994[1]. To keep the customer ahead of the competition, Intel has developed four new proliferations, the Cobra series of the i960 processor family. These give the engineer the ability to design for the future while keeping system costs low.

The Cobra series members are differentiated by frequency, core speed, operation voltage and cache size. The first proliferation, the 80960JF, utilizes 4-Kbyte, 2-way set associative instruction cache, 2-Kbyte direct mapped data cache at 5V and 3V. The 80960JA will have 2-Kbyte instruction cache and 1-Kbyte data cache at 5V and 3V. The highest proliferation, the 80960JD, will contain 4-Kbyte instruction cache, 2-Kbyte data cache plus an internal clock doubler. Since the Cobra series is object code compatible with the entire i960 processor family and will be supported by the full range of independent software, hardware, and development tool vendors, your software investment from prior i960 processor based designs will be preserved and ease-of-design increased.

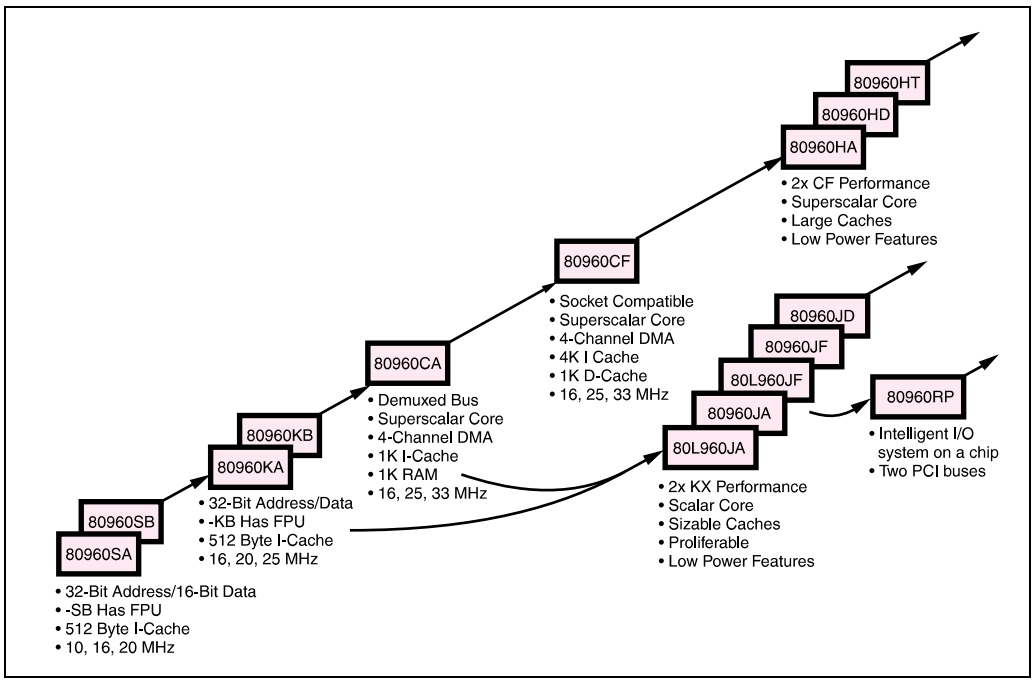
THE COBRA PROCESSOR SERIES

Using the latest in technology enhancements, Intel has created a series of microprocessors offering new levels of power and performance. What does that mean to the engineer? It means more performance with less power. It means sustained, one instruction per clock cycle performance. It means that you get power consumption of less than one watt. Finally, it means that the 80960JF-33 MHz microprocessor of the Cobra series produces 31 VAX MIPS.

The new Cobra series will also help reduce system cost. Intel has kept in mind the cost and anxiety of converting from one architecture to another or from one product to another without any compatibility. The Cobra series will be code compatible with the entire i960 processor family, saving in development tool costs, design costs and time to market.

	Instruction Cache Size	Data Cache Size	Power	Speed Doubler	Product
80960JA	2K I-cache	1K D-cache	5V	No	Base version at 5V of the P100 architecture
80L960JA	2K I-cache	1K D-cache	3.3V	No	Base version at 3.3V of the P100 architecture
80L960JF	4K I-cache	2K D-cache	3.3V	No	2 x the cache size of the base version at 3.3V
80960JF	4K I-cache	2K D-cache	5V	No	2 x the cache size of the base version at 5V
80960JD	4K I-cache	2K D-cache	5V	Yes	2 x the cache size with speed doubler technology at 5V

[1] Source: DataQuest

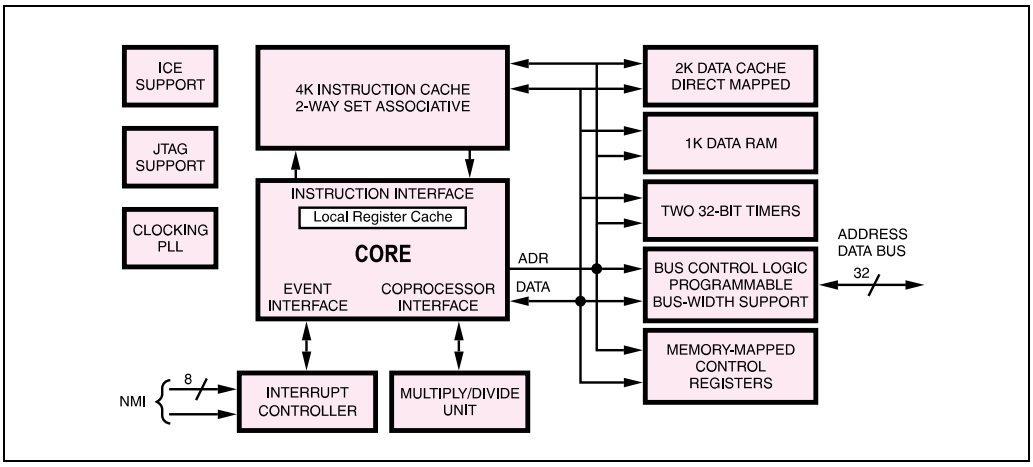


i960® Microprocessor Family Road Map

The i960 Jx processor series offers many benefits, number one is pin-for-pin compatibility. Upgradability plays a significant role in system cost and time-to-market. With the Cobra series, it is possible to have one design that produces four different products with four different levels of performance.The newest members of the i960 processor family offer other features: an i960 processor compatible RISC core, power consumption at 3.3V and 5V, halt mode and advanced cache memory at many levels of performance. All of these features help mold designers applications to fit specific markets.

PRODUCT HIGHLIGHTS

- i960 processor-compatible RISC core
- 45 MIPS execution for the 80960JD50
- 4 Kbyte two-way set associative instruction cache
- 2 Kbyte direct mapped data cache
- 1 Kbyte on-chip data RAM
- Built-in interrupt controller
- 2X internal mode clock (80960JD version only)
- KA processor compatible external bus and i960 CA processor compatible programmable bus width support
- Two 32-bit timers



i960® Jx Processor Block Diagram

FEATURES	BENEFITS
▪ Pin-for-pin compatibility for all versions of the Cobra series processors	▪ Quick, easy design upgrades
▪ High performance embedded architecture - 45 MIPS per watt execution at 50 MHz	▪ More performance, less power, lower system cost
▪ 4-Kbyte on-chip instruction cache - 2-way set associative - Cache lock modes	▪ Reduces external bus traffic, accelerates execution of standard software and time-critical interrupt routines
▪ 2-Kbyte data cache - Direct mapped, write through	▪ Enhances performance to maintain single-cycle instruction issue
▪ 32-bit multiplexed burst bus - Bus width is programmable by region, 8-, 16-,or 32-bits wide - Compatible with the 80960KA L-Bus - Supports bursts up to four 32-bit words	▪ System cost reduction and compatibility with the 80960KA L-bus
▪ Supports aligned/unaligned big or little endian accesses - Multiword unaligned big endian	▪ Able to read aligned/unaligned words without system degradation or performance losses
▪ Two identical 32-bit timers - Fully independent with auto-reload	▪ Reduces board level cost with integration and reduces chip count
▪ Local register cache - 8 local register sets - Saves or restores 16 local registers in 4 clock cycles - 128-bit wide interface for quick context switches on call, returns and interrupts	▪ Fast context switching for critical routines, which reduces the external bus traffic
▪ JTAG - Supports IEEE 1149.1 standards	▪ Makes testing and debugging of surface mount systems possible through a common JTAG standard
▪ High speed interrupt controller - 8 maskable external interrupt pins - One non-maskable interrupt pin - Two internal timer sources - Programmable edge or level detection - 248 interrupt vectors	▪ Improves control. Prioritization of software interrupts, hardware interrupts and the process priority.
▪ Low power - As much as a 50% power reduction from i960 CF processor	▪ Enables more performance with less powerconsumption
▪ Power management features - Halt mode - 80% power reduction during HALT	▪ Lowers power use during inactive period to meet office environment

NETWORKING APPLICATIONS

From SCSI cards to bridges to routers and hubs, the Cobra series is well adapted to handle intelligent I/O design. In applications requiring the crossing over from one data stream to another, typical in ATM_to_FDDI designs, the byte swapping capability of these new processors gives the designer a new range of flexible solutions.

The i960 JF microprocessor has added instruction cache to keep external accesses to a minimum, increasing processing performance of the actual application. Low power, halt mode and special internal feature management techniques are used to reduce power consumption by shutting down inactive units. All of these features may help lower system cost by eliminating fans and board space. Peripheral chips and software solutions are available from National, Brooktree, Router Engine and STAC to provide cost-effective networking solutions for the customer. These peripherals include:

- National SONIC Ethernet coprocessor
- Brooktree Bt8220 ATM receiver/transmitter
- Brooktree UGA-210 SMDS control and reassembly formatter
- Router Engine iFX780 FLEXlogic FPGA DRAM controller
- STAC LZS221-960 lossless compression software

IMAGING APPLICATIONS

The i960 microprocessor family offers an optimum performance solution for page-printing applications. A single design based on one of the four Cobra series processors can span performance requirements from 5 ppm to 35 ppm and support resolutions up to 1200 dpi. Portable applications can use the i960 JF processor design, with the two 3V versions and inclusion of special power management features. Since the Cobra series processors are software- and pin-compatible, the system designer can offer a variety of price/performance platforms while allowing for future performance upgrades. This design flexibility affords the system manufacturer faster time-to-market while amortizing system design costs across multiple platforms.

The i960 JF microprocessor's external bus is compatible with the printer industry-standard i960 KA/KB microprocessors. This ensures compatibility with a vast array of peripheral coprocessor chips that are already available. These include the Intel 82961KD and solutions from members of the Solutions 960® program such as Destiny Technology Corporation and Topmax (TDS).

Intel Reference Numbers	
FaxBack System:	1 (800) 628-2283 or (916) 356-3105
Application Bulletin Board System:	(916) 356-3600
Other Intel Support Intel Literature Center:	1 (800) 548-4725 7 a.m. to 7 p.m. CST
Retail PC and Network Products:	1 (800) 538-3373 or (503) 629-7000 7 a.m. to 7 p.m. PST
General Information Hotline:	1 (800) 628-8686 & (916) 356-3104 5 a.m. to 5 p.m. PST
World Wide Web Address:	http://www.intel.com/embedded/

UNITED STATES
Intel Corporation
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA
95052-8119

JAPAN
Intel Japan, K.K.
5-6 Tokodai,
Tsukuba-shi
Ibaraki
300-26

FRANCE
Intel Corporation
S.A.R.L.
1, Rue Edison, BP 303
78054, Saint Quentin-en-Yvelines Cedex

UNITED KINGDOM
Intel Corporation
(U.K.) Ltd.
Pipers Way
Swindon
Wiltshire, England
SN3 1RJ

GERMANY
Intel GmbH
Dornacher Strasse 1
85622
Feldkirchen/Muenchen

HONG KONG
Intel Semiconductor Ltd.
32/F Two Pacific Place
88 Queensway
Central

CANADA
Intel Semiconductor of Canada, Ltd.
190 Attwell Drive,
Suite 500
Rexdale, Ontario
M9W 6H8

Printed on Recycled Paper

Order Number 272506-002 Printed in U.S.A./695/10K/IL KG